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EXAMINER	
WANG, JIN CHENG	
ART UNIT	**PAPER NUMBER**
2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,913	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's submissions filed on 06/23/2005 has been entered. Claim 1, 6, 11, 16, 20 have been amended. Claims 1-27 are pending in the application.

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are not found persuasive in view of the ground(s) of rejection based on Odryna et al. U.S. Pat. No. 6,333,750 (hereinafter Odryna) in view of Glen U.S. Patent No. 6,157,415 (Glen-415) and Glen U.S. Patent No. 6,268,847 (hereinafter Glen-847).

For example, Odryna teaches a plurality of digital decoders configured to digitally decode a plurality of image signals wherein each of the plurality of digital decoder incorporated in each of the input cards, Input A, Input B, Input C of Figure 17. Each of the input card as shown in Figure 21 has a digital decoder 182; see column 15-22.

Odryna further teaches an image selector wherein a combination of control elements and memories within the circuit blocks of Fig. 17 constitutes an image selector. For example, the combination of the set of discrete elements such as the control block 111 shown in Fig. 18 within the system card 110 of Fig. 17, the serial control bus 113 of Figs. 18 and 21, the control array 188 and the memories 186 shown in Fig. 21 within the Input A, or Input B, or Input C of Fig. 17 constitutes the image selector. This is because the control block 111 interconnected and bi-directionally communicates with the serial control bus 113 and the control array 188 and memories 186 interconnected and bi-directionally communicate with the serial control bus 113.

The plurality of circuit elements forms an integral control block that constitutes an image selector. The integral control block is responsible for issuing the instructions for the overlay of the image layers; see column 17. It also controls the control gate arrays within the other input cards wherein each of the control gate arrays is programmed via the serial control buses 113; see column 21. Note that all the control gate arrays are programmed by the control block 111 of the system card 110 via the serial control bus 113 to control the overlay of the base image with other images. Odryna thus teaches that the outputs of the decoder 182 are directly sent to the image selector comprising the control array 188 of Fig. 21 and the control block 111 of Fig. 18.

Odryna teaches a plurality of resolution converters in which the ***scaler 184 of Figure 21*** *scales the input image and the common control gate array 120 within the system card 110 together with the pixel bus 114 defines how an overlay window is established (column 18, lines 1-15) and thus controls the display resolution. Therefore, the resolution of the input image is controlled by the scaler 184 of each input card, the control gate array 120 of the system card 110 which controls the resolution of the overlay window associated with each input image through the pixel bus 114. The discrete elements performs a resolution conversion.* In column 20-21, Odryna teaches another embodiments of the BVIDEO overlay card of Fig. 21 wherein the scaler 184 is utilized at the output of the buffer memory 186 and therefore the scaler 184 and the control gate array 120 together with the pixel bus 114 as a whole directly receives image data outputs from the buffer memory 186 which are controlled by the control gate array 188. Odryna teaches a resolution converter within each of the input cards shown in Fig. 17 because the resolution converter (scaler 184) directly receives image data outputs from the image selector comprising the buffer memory 186 and the control gate array 188 as well as the control block

111 and serial control bus 113. Moreover, Odryna teaches a plurality of the resolution converters because each of the plurality of the input cards, Input A, Input B, Input C of Fig. 17 has a scaler 184 together with the control gate array 120 and the pixel bus 114 which controls the resolution of the window overlay from each of the input sources.

Therefore, Odryna does disclose a set of plurality of discrete control elements to be used for the image selection of the plurality of output image signals from the digital decoders.

Although Odryna did not specifically teach that an image selector is made of the plurality of discrete elements for the construction of an integral control block as an image selector, it is well known to one of the ordinary skill in the art to have made an integral element out of those bi-directly communicable and interconnected discrete circuit elements of Odryna to form the integral control block. See *In re Larson*, 144 USPQ 347, 349; 339 US 965 (CCPA 1965) and *In re Wolfe*, 116 USPQ 443, 444; 251 F2d 854 (CCPA 1958).

One having the ordinary skill in the art would have been motivated to do this because it would have provided an integral block out of a set of bi-directly communicable and interconnected discrete circuit elements.

Odryna is silent to the claim limitation of "the image selector is configured to connect each of the digital decoders to any of the resolution converters." However, *Odryna teaches a plurality of resolution converters in which the **scaler 184 of Figure 21** scales the input image and the common control gate array 120 within the system card 110 together with the pixel bus 114 defines how an overlay window is established (column 18, lines 1-15) and thus controls the display resolution. Therefore, the resolution of the input image is controlled by the scaler 184 of each input card, the control gate array 120 of the system card 110 which controls the resolution*

of the overlay window associated with each input image through the pixel bus 114. The discrete elements perform a resolution conversion for each of the input image signal from each of the input card. In column 20-21, Odryna teaches another embodiments of the BVIDEO overlay card of Fig. 21 wherein the scaler 184 is utilized at the output of the buffer memory 186 and therefore the scaler 184 and the control gate array 120 together with the pixel bus 114 as a whole directly receives image data outputs from the buffer memory 186 which are controlled by the control gate array 188. Odryna teaches a resolution converter within each of the input cards shown in Fig. 17 because the resolution converter (scaler 184) directly receives image data outputs from the image selector comprising the buffer memory 186 and the control gate array 188 as well as the control block 111 and serial control bus 113. Moreover, Odryna teaches a plurality of the resolution converters because each of the plurality of the input cards, Input A, Input B, Input C of Fig. 17 has a scaler 184 together with the control gate array 120 and the pixel bus 114 which controls the resolution of the window overlay from each of the input sources. The pixel bus 114 as controlled by the control gate array 120 together with the scaler 184 of each input card acts as a resolution converter for converting the resolution of the overlay window for each of the input sources from each of the input cards. Each input source is directed to the pixel bus 114 which defines the resolution of the overlay window using the control gate array 120's instructions and thus there is a common resolution converter for converting the resolution for each of the input sources.

Applicant argues that a claim element set forth in the claim 1 requires each resolution converter can input any of the respective outputs. However, the scaler 184 receives any of the *respective outputs* from the image selector through the instructions from the control array 188 and the system card. Moreover, one input card may receive output from another input card so

that further overlaid windows could be merged into the pixel data (see column 21, lines 40-67 and column 22, lines 1-17). The scaler 184 of one input card can receive output from another input card through **the data exchange module 200** wherein the data handling unit 210 further reformat the pixel data into the desired output format (resolution conversion of the pixel data). Thus, the scaler 184 receives any of the respective outputs from the image selector through the data exchange module 200. Finally, applicant has not particularly pointed out the claim limitation of "any of the respective outputs" because any of the respective outputs may refer to any of the respective outputs from the respective decoders. In this sense, Odryna's scaler 184 receives any of the respective outputs from the respective decoders without even using the data exchange module 200. The functionality of applicant's claim invention is to achieve resolution conversion for any of the input sources. Applicant is trying to argue that a different circuit configuration has been claimed in the claim invention set forth in the claim 1. Even for the argument's sake that applicant's circuit configuration may differ from Odryna's circuit, applicant, however, did not provide any support that applicant's claim invention achieves more functionality than Odryna's invention. In this regards, the other cited reference provide different circuit configurations to achieve the same functionality as applicant's claim invention set forth in the claim 1.

For example, in Fig. 9, Glen teaches "the image selector is configured to connect each of the digital decoders to any of the resolution converters" wherein the image selector is the switch matrix 140 and the resolution converters are the color base converting module 102, blend module 76, 78 and 80. As regards to the embodiment of Fig. 9, Glen-847 in column 1, lines 25-39 teaches incorporating video decoders and video capture module for processing TV signals and

therefore the combination of Glen-415's Fig. 9 and Glen-847's teaching discloses that decoders are incorporated into Fig. 9 for processing the analog TV input signals and HDTV input signals to convert to digital representations to the switch matrix 140.

Glen-415 inherently teaches a plurality of digital decoders within any color base-converting module. This is because a color base converter necessarily provides a set of decoders (such as address decoders) for decoding bits/pixel. Therefore, Glen-415 teaches resolution converters that receive as input the color converted signals from any of the color base-converting module. The configuration module 40 of figure 8, for example, determines which output signals from the color converting modules are selected. Therefore, Glen-415 teaches an image selector (such as the configuration module 40) selects from among the plurality of digitally decoded image signals that are digitally decoded by a plurality of digital decoders (by a plurality of the color base-converting modules). Notice that Glen-415 teaches a plurality of color base-converting modules in the image-processing device with each of the modules having a plurality of digital decoders.

In figures 7-9, Glen-415 teaches programmable blending module 116 (which functions as a plurality of blending modules set forth in figures 6A-6C) and configuration module 40 (which functions as an image selector corresponding to applicant's claimed invention). It is clearly shown in Figures 7 and 8 that the blending module receives as input any of the signals output from a selector (i.e., the configuration module 40) in combination with the multiplexers 110/112/114.

Moreover, Glen-415 further discloses the blending modules adjust the resolutions of the selected output signals (Glen-415 column 8, lines 50-60).

Therefore, it would have been obvious to one of ordinary skill in the art to have incorporated a different circuit configuration in whatever form such as a different configuration as configured in other cited reference, for example, the circuit configuration of the Glen-415 reference wherein the image selector is used to connect each of the decoder output signals or the input image signals to any of the resolution converter, into Odryna's system because Odryna's system is highly reconfigurable with instructions from the programmable controller such as the system card. Odryna also teaches the image selector which selects an output from one of the decoder to direct to one of the resolution converters so that overlaying data can be merged into the base image on the pixel bus 114 on a pixel-by-pixel basis or according to various algorithms pre-programmmed into the local control gate array. Moreover, the control array 120 defines the size of the overlay window for each input source and thus controls the resolution of each overlay window (Odryna column 18-21; column 15-16) and one input card can receive output from another input card through the data exchange module (Odryna column 21-22).

One having the ordinary skill in the art would have been motivated to do this because it would have provided a switching scheme for the conversion of the image output signals from one of the decoders and have provided a different circuit configuration and for the subsequent multistage synthesis for overlaying the portions of the input images (Glen-415 column 3-4 and Odryna column 21-22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Odryna et al. U.S. Pat. No. 6,333,750 (hereinafter Odryna), in view of Glen U.S. Patent No. 6,157,415 (Glen-415) and Glen U.S. Patent No. 6,268,847 (hereinafter Glen-847).

1. Re Claims 1 and 6:

(a) Odryna teaches an overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2, the overlay image processing device comprising:

A plurality of digital decoders configured to digitally decode a plurality of image signals (*e.g., each of the plurality of digital decoder incorporated in each of the input cards, Input A, Input B, Input C of Figure 17 wherein the input cards, Input A or Input B or Input C of Figure 17 are shown in Figure 21 with each input card having a digital decoder 182 of Fig. 21; see column 15-22*);

An image selector (*A combination of control elements and memories within the circuit blocks of Fig. 17 constitutes an image selector. For example, the combination of the control block 111 shown in Fig. 18 within the system card 110 of Fig. 17, the control array 188 and the memories 186 shown in Fig. 21 within the Input A, or Input B, or Input C of Fig. 17 constitutes the image selector. This is because the control block 111 is responsible for issuing the instructions for the overlay of the image layers; see column 17. It also controls the control gate arrays within the other input cards wherein each of the control gate arrays is programmed via*

the serial control buses; see column 21. Note that all the control gate arrays are programmed by the control block 111 of the system card 110 via the serial control bus to control the overlay of the base image with other images) configured to directly receive outputs from each of the plurality of digital decoders (*the outputs of the decoder 182 are directly sent to the image selector comprising the control array 188 and the memories 186 of Fig. 21 and the control block 111 of Fig. 18*) and configured to select from among a plurality of digitally decoded image signals one reference image signal (the base image) and (n-1) number of superimposing image signals (See, column 15-25);

A plurality of resolution converters (*The **scaler 184 of Figure 21** meets the claim limitation of a resolution converter because column 20-21 of Odryna teaches another embodiments of the BVIDEO overlay card of Fig. 21 wherein the scaler 184 is utilized at the output of the buffer memory 186 and the scaler 184 directly receives image data outputs from the buffer memory 186 which are controlled by the control gate array 188. Odryna teaches a plurality of resolution converters because each of the plurality of the input cards, Input A, Input B, Input C of Fig. 17 has a scaler 184*) configured to directly receive the selected image signals output from the image selector, to convert resolutions of the n number of selected image signals into respective adjustable desired resolutions (column 20-21), and to output the converted image signals to an image synthesizer (the pixel bus 114 constitutes an image synthesizer performing overlaying operation on a pixel-by-pixel basis; see for example, column 20, lines 15-20; column 15, lines 58-67; column 21, lines 1-8; column 16, lines 1-15),

wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal (e.g., column 20, lines 15-20; column 15, lines 58-67; column 16, lines 1-15).

In other words, Odryna teaches a plurality of digital decoders configured to digitally decode a plurality of image signals wherein each of the plurality of digital decoder incorporated in each of the input cards, Input A, Input B, Input C of Figure 17. Each of the input card as shown in Figure 21 has a digital decoder 182; see column 15-22.

Odryna further teaches an image selector wherein a combination of control elements and memories within the circuit blocks of Fig. 17 constitutes an image selector. For example, the combination of the set of discrete elements such as the control block 111 shown in Fig. 18 within the system card 110 of Fig. 17, the serial control bus 113 of Figs. 18 and 21, the control array 188 and the memories 186 shown in Fig. 21 within the Input A, or Input B, or Input C of Fig. 17 constitutes the image selector. This is because the control block 111 interconnected and bi-directionally communicates with the serial control bus 113 and the control array 188 and memories 186 interconnected and bi-directionally communicate with the serial control bus 113. The plurality of circuit elements forms an integral control block that constitutes an image selector. The integral control block is responsible for issuing the instructions for the overlay of the image layers; see column 17. It also controls the control gate arrays within the other input cards wherein each of the control gate arrays is programmed via the serial control buses 113; see column 21. Note that all the control gate arrays are programmed by the control block 111 of the system card 110 via the serial control bus 113 to control the overlay of the base image with other

images. Odryna thus teaches that the outputs of the decoder 182 are directly sent to the image selector comprising the control array 188 of Fig. 21 and the control block 111 of Fig. 18.

However, *Odryna teaches a plurality of resolution converters in which the* ***scaler 184 of Figure 21*** *scales the input image and the common control gate array 120 within the system card 110 together with the pixel bus 114 defines how an overlay window is established (column 18, lines 1-15) and thus controls the display resolution. Therefore, the resolution of the input image is controlled by the scaler 184 of each input card, the control gate array 120 of the system card 110 which controls the resolution of the overlay window associated with each input image through the pixel bus 114. The discrete elements perform a resolution conversion for each of the input sources from each of the input cards*. In column 20-21, Odryna teaches another embodiments of the BVIDEO overlay card of Fig. 21 wherein the scaler 184 is utilized at the output of the buffer memory 186 and therefore the scaler 184 and the control gate array 120 together with the pixel bus 114 as a whole directly receives image data outputs from the buffer memory 186 which are controlled by the control gate array 188. Odryna teaches a resolution converter within each of the input cards shown in Fig. 17 because the resolution converter (scaler 184) directly receives image data outputs from the image selector comprising the buffer memory 186 and the control gate array 188 as well as the control block 111 and serial control bus 113. Moreover, Odryna teaches a plurality of the resolution converters because each of the plurality of the input cards, Input A, Input B, Input C of Fig. 17 has a scaler 184 together with the control gate array 120 and the pixel bus 114 which controls the resolution of the window overlay from each of the input sources. The pixel bus 114 as controlled by the control gate array 120 together with the scaler 184 of each input card acts as a resolution converter for converting the resolution

of the overlay window for each of the input sources. Each input source is directed to the pixel bus 114 which defines the resolution of the overlay window using the control gate array 120's instructions and thus there is a common resolution converter for converting the resolution for each of the input sources.

(b) Odryna does disclose a set of plurality of discrete control elements to be used for the image selection of the plurality of output image signals from the digital decoders.

(c) Although Odryna did not specifically teach that an image selector is made of the plurality of discrete elements for the construction of an integral control block as an image selector, it is well known to one of the ordinary skill in the art to have made an integral element out of those bi-directly communicable and interconnected discrete circuit elements of Odryna to form the integral control block. See *In re Larson*, 144 USPQ 347, 349; 339 US 965 (CCPA 1965) and *In re Wolfe*, 116 USPQ 443, 444; 251 F2d 854 (CCPA 1958).

(d) One having the ordinary skill in the art would have been motivated to do this because it would have provided an integral block out of a set of bi-directly communicable and interconnected discrete circuit elements.

(e) However, Odryna is silent to the claim limitation of "the image selector is configured to connect each of the digital decoders to any of the resolution converters." However, *Odryna teaches a plurality of resolution converters in which the* ***scaler 184 of Figure 21*** *scales the input image and the common control gate array 120 within the system card 110 together with the pixel bus 114 defines how an overlay window is established (column 18, lines 1-15) and thus controls the display resolution. Therefore, the resolution of the input image is controlled by the scaler 184 of each input card, the control gate array 120 of the system card 110 which controls the*

resolution of the overlay window associated with each input image through the pixel bus 114. The discrete elements perform a resolution conversion for each of the input sources from each of the input cards. In column 20-21, Odryna teaches another embodiments of the BVIDEO overlay card of Fig. 21 wherein the scaler 184 is utilized at the output of the buffer memory 186 and therefore the scaler 184 and the control gate array 120 together with the pixel bus 114 as a whole directly receives image data outputs from the buffer memory 186 which are controlled by the control gate array 188. Odryna teaches a resolution converter within each of the input cards shown in Fig. 17 because the resolution converter (scaler 184) directly receives image data outputs from the image selector comprising the buffer memory 186 and the control gate array 188 as well as the control block 111 and serial control bus 113. Moreover, Odryna teaches a plurality of the resolution converters because each of the plurality of the input cards, Input A, Input B, Input C of Fig. 17 has a scaler 184 together with the control gate array 120 and the pixel bus 114 which controls the resolution of the window overlay from each of the input sources. The pixel bus 114 as controlled by the control gate array 120 together with the scaler 184 of each input card acts as a resolution converter for converting the resolution of the overlay window for each of the input sources. Each input source is directed to the pixel bus 114 which defines the resolution of the overlay window using the control gate array 120's instructions and thus there is a common resolution converter for converting the resolution for each of the input sources.

Moreover, one input card may receive output from another input card so that further overlaid windows could be merged into the pixel data (see column 21, lines 40-67 and column 22, lines 1-17). The scaler 184 of one input card can receive output from another input card through **the data exchange module 200** wherein the data handling unit 210 further reformat the

pixel data into the desired output format (resolution conversion of the pixel data). Thus, the scaler 184 receives any of the respective outputs from the image selector through the data exchange module 200. Odryna's scaler 184 also receives any of the respective outputs from the respective decoders without even using the data exchange module 200.

(f) In Fig. 9, Glen-415 teaches "the image selector is configured to connect each of the digital decoders to any of the resolution converters" wherein the image selector is the switch matrix 140 and the resolution converters are the color base converting module 102, blend module 76, 78 and 80. As regards to the embodiment of Fig. 9, Glen-847 in column 1, lines 25-39 teaches incorporating video decoders and video capture module for processing TV signals and therefore the combination of Glen-415's Fig. 9 and Glen-847's teaching discloses that decoders are incorporated into Fig. 9 for processing the analog TV input signals and HDTV input signals to convert to digital representations to the switch matrix 140.

With regards to the other embodiments, Glen-415 further teaches an overlay image processing device (e.g., figures 2, 7-9) for generating an overlay image signal composed of an n number of superimposed image signals, n being an integer greater than 2, the overlay image processing device comprising:

A plurality of digital decoders configured to digitally decode a plurality of image signals (e.g., the decoders are inherently incorporated into color base conversion module 42, 44, and 46 of figures 2, 7-8. column 11, lines 1-67; column 12, lines 1-45);

An image selector (e.g., the input select 106 of figures 6A-6C/convert select 104 of figures 6A-6C/control 60 of the configuration module 40 in figures 2, 7-9; see also column 3, lines 35-67; column 4, lines 1-55) configured to directly receive outputs from each of the

plurality of digital decoders and configured to select from among a plurality of digitally decoded image signals one reference image signal and (n-1) number of superimposing image signals (See, for example, figures 6-8; column 8, lines 4-15);

A plurality of resolution converters (e.g., blending module 48 and 50 being similar to the programmable blending module 116 performing resolution conversion function. See figures 7-9, column 8, lines 45-60) configured to directly receive the selected image signals output from the image selector, such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective desired resolutions, and to output the converted image signals to an image synthesizer (e.g., figures 2-9; column 8, lines 45-60); and

An image synthesizer (e.g., blend module 76, 78 and 80 of figure 3 and 9) configured to superimpose the (n-1) number of converted superimposing image signals on the converted reference signal (e.g., figures 2-9; column 6, lines 15-45).

Glen-415 inherently teaches a plurality of digital decoders within any color base-converting module. This is because a color base converter necessarily provides a set of decoders (such as address decoders) for decoding bits/pixel. Therefore, Glen-415 teaches resolution converters that receive as input the color converted signals from any of the color base-converting module. The configuration module 40 of figure 8, for example, determines which output signals from the color converting modules are selected. Therefore, the examiner asserts that Glen-415 teach an image selector (such as the configuration module 40) selects from among the plurality of digitally decoded image signals that are digitally decoded by a plurality of digital decoders (by a plurality of the color base-converting modules). Notice that Glen-415 teaches a plurality of

color base-converting modules in the image-processing device with each of the modules having a plurality of digital decoders.

In figures 7-9, Glen-415 teaches programmable blending module 116 (which functions as a plurality of blending modules set forth in figures 6A-6C) and configuration module 40 (which functions as an image selector corresponding to applicant's claimed invention). It is clearly shown in Figures 7 and 8 that the blending module receives as input any of the signals output from a selector (i.e., the configuration module 40) in combination with the multiplexers 110/112/114.

Moreover, Glen-415 further discloses the blending modules adjust the resolutions of the selected output signals (Glen-415 column 8, lines 50-60).

(g) Therefore, it would have been obvious to one of ordinary skill in the art to have incorporated a different circuit configuration in whatever form such as a different configuration as configured in other cited reference, for example, the circuit configuration of the Glen-415 reference wherein the image selector is used to connect each of the decoder output signals or the input image signals to any of the resolution converter, into Odryna's system because Odryna's system is highly reconfigurable with instructions from the programmable controller such as the system card. Odryna also teaches the image selector which selects an output from one of the decoder to direct to one of the resolution converters so that overlaying data can be merged into the base image on the pixel bus 114 on a pixel-by-pixel basis or according to various algorithms pre-programmmed into the local control gate array. Moreover, the control array 120 defines the size of the overlay window for each input source and thus controls the resolution of each overlay

window (Odryna column 18-21; column 15-16) and one input card can receive output from another input card through the data exchange module (Odryna column 21-22).

(h) One having the ordinary skill in the art would have been motivated to do this because it would have provided a switching scheme for the conversion of the image output signals from one of the decoders and have provided a different circuit configuration and for the subsequent multistage synthesis for overlaying the portions of the input images (Glen-415 column 3-4 and Odryna column 21-22).

Claim 2:

The claim 2 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of at least one of the plurality of image signals being a display signal output from a personal computer. However, Odryna further discloses the claimed limitation of at least one of the plurality of image signals being a display signal output from a personal computer (e.g., column 18).

Claim 3:

The claim 3 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

However, Odryna further discloses the claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition (e.g., figures 17-21; column 15-25).

Claim 4:

The claim 4 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of a scan converter configured to convert at least one of the interlaced image signals selected by the image selector into a non-interfaced image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

However, Odryna further discloses the claimed limitation of a scan converter configured to convert at least one of the interlaced image signals selected by the image selector into a non-interfaced image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal (e.g., figures 17-21; column 15-25).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of at least one of the plurality of image signals being a display signal output from a personal computer. However, Odryna further discloses the claimed limitation of at least

one of the plurality of image signals being a display signal output from a personal computer (e.g., column 18).

Claim 8:

The claim 8 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition. However, Odryna further discloses the claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition (figures 17-21; column 15-25).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 6 except additional claimed limitation identical to that set forth in claim 4. The claim 9 is rejected for the same reason set forth in claim 4.

2. Claims 11-14:

Each of the claims 11-14 is a rephrasing of the claims 1-4 respectively in a method form. The claims are rejected for the same reason as set forth above.

3. Claims 16-19:

Each of the claims 16-19 encompasses the same scope of invention as that of claims 1-4. The claims are subject to the same rationale of rejection set forth in claims 1-4.

4. Claims 20-23:

Each of the claims 20-23 is a rephrasing of the claims 16-19 respectively in a method form. The claims are rejected for the same reason as set forth above.

Claim 5:

(1) The claim 5 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the image synthesizer having the n number of 2-input image synthesizers, each 2-input image synthesizer being configured to receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal; the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of ith stage, where I is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of (I –1)th stage as the lower-side image signal and ith superimposing image signal as the upper-side image signal.

However, Glen-415 further discloses the claimed limitation of the image synthesizer having the n number of 2-input image synthesizers, each 2-input image synthesizer being

configured to receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal; the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of ith stage, where I is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of (I –1)th stage as the lower-side image signal and ith superimposing image signal as the upper-side image signal (Glen-415 figures 5, 6 and 9, and column 3, lines 51-65).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 6 except additional claimed limitation identical to that set forth in claim 5. The claim 10 is rejected for the same reason set forth in claim 5.

Claim 15:

The claim 15 is a rephrasing of the claim 5 respectively in a method form. The claims are rejected for the same reason as set forth above.

Claim 24-25:

(1) The claim 24 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the respective outputs of the image selector include an analog RGB signal and a horizontal sync signal, wherein each of the resolution converters generates a

clock signal synchronized with the horizontal sync signal and corresponding to a pixel clock for the analog RGB signal, and quantizes the RGB signal in synchronism with the clock signal to convert the analog RGB signal to a digital RGB signal, and wherein a single image signal element quantized by each of the resolution converters corresponds to one pixel of the image represented by the RGB signal.

(2) Odryna teaches the limitation set forth in the claim 6. However, Odryna's teaching of the resolution converter is configured by separating functionality of image decoding and resolution converting.

(3) Odryna teaches the image decoder for converting analog RGB signal to a digital RGB signal wherein the image decoder and the scaler of Figure 21 meets the claim limitation recited in claim 24.

(4) It would have been obvious to one of ordinary skill in the art to have moved some functionality from the image decoder into the resolution converter of Odryna because the circuits of the image decoder can be reconfigured and therefore by incorporating some of the reconfigured circuits into the scaler of Figure 21 of Odryna a new resolution converter can be constructed.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a resolution converter with additional functionalities.

Claim 25:

The claim 25 is subject to the same rationale of rejection set forth in the claim 24.

Claim 26:

The claim 26 is subject to the same rationale of rejection set forth in the claim 24.

Claim 27:

The claim 27 is subject to the same rationale of rejection set forth in the claim 24.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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